What is claimed is:

1. A stacked gate vertical flash memory, comprising:
a semiconductor substrate with a trench;
a source conducting layer, formed on a bottom of the trench;
an insulating layer, formed on the source conducting layer;
a gate dielectric layer, formed on a sidewall of the trench;
a conducing spacer, formed on the gate dielectric layer as a floating gate;
an inter-gate dielectric layer, covered on the conducting spacer; and
a conducting control gate filled in the trench.

2. The stacked gate vertical flash memory as claimed in claim 1, wherein the source conducting layer comprises a polysilicon layer or an epi-silicon layer

3. The stacked gate vertical flash memory as claimed in claim 2, wherein the source conducting layer is a doped As ion layer.

4. The stacked gate vertical flash memory as claimed in claim 1, wherein the source conducting layer can be a common source.

5. The stacked gate vertical flash memory as claimed in claim 1, wherein the insulating layer comprises an oxide layer.

6. The stacked gate vertical flash memory as claimed in claim 1, wherein the gate dielectric layer comprises a gate oxide layer.

7. The stacked gate vertical flash memory as claimed in claim 1, wherein the top portion of the conducting spacer is a tip.

8. The stacked gate vertical flash memory as claimed in claim 1, wherein the conducting spacer comprises a polysilicon layer or an epi-silicon layer.

9. The stacked gate vertical flash memory as claimed in claim 1, wherein the inter-gate dielectric layer comprises a gate oxide layer.

10. The stacked gate vertical flash memory as claimed in claim 1, wherein the second conducting layer comprises a polysilicon layer or an epi-silicon layer.

11. The stacked gate vertical flash memory as claimed in claim 1, further comprises a source area formed on a side of the insulating layer in the semiconductor substrate, wherein the source comprises an As ion implanted area.

12. The stacked gate vertical flash memory as claimed in claim 1, further comprises a drain area formed on a side of the top of the conducting spacer in the semiconductor substrate, wherein the drain comprises an As ion implanted area.

13. The stacked gate vertical flash memory as claimed in claim 1 further comprises an isolation oxide layer for

separating the source conducting layer and the semiconductor substrate.

14. A stacked gate vertical flash memory, comprising:

a semiconductor substrate with a trench, wherein an isolation layer is formed on a bottom of the trench;

a source conducting layer, formed on the bottom of the trench, wherein the source conducting layer and the semiconductor substrate are separated by the isolation layer;

an insulating layer, formed on the source conducting layer, wherein the insulating layer and others formed thereon are separated by the insulating layer;

a gate dielectric layer, formed on a sidewall of the trench;

a conducing spacer, formed on the gate dielectric layer as a floating gate;

a source area, formed on a side of the insulating layer in the semiconductor substrate, wherein the conducting spacer electrically connected to the source conducting layer and the conducting spacer;

a drain area, formed on a side of a top of the conducting spacer;

an inter-gate dielectric layer, covered on the conducting spacer; and

a control gate conducting filled in the trench.

15. The stacked gate vertical flash memory as claimed in claim 14, wherein the source conducting layer comprises a polysilicon layer or an epi-silicon layer

16. The stacked gate vertical flash memory as claimed in claim 14, wherein the source conducting layer is an As ion doped layer.

17. The stacked gate vertical flash memory as claimed in claim 14, wherein the insulating layer comprises an oxide layer.

18. The stacked gate vertical flash memory as claimed in claim 14, wherein the gate dielectric layer comprises a gate oxide layer.

19. The stacked gate vertical flash memory as claimed in claim 14, wherein the top portion of the conducting spacer is a tip.

20. The stacked gate vertical flash memory as claimed in claim 14, wherein the conducting spacer comprises a polysilicon layer or an epi-silicon layer.

21. The stacked gate vertical flash memory as claimed in claim 14, wherein the source conducting layer can be an As ion doped layer.

22. The stacked gate vertical flash memory as claimed in claim 14, wherein the drain conducting layer can be an As ion doped layer.

23. The stacked gate vertical flash memory as claimed in claim 14, wherein the inter-gate dielectric layer comprises a gate oxide layer.

24. The stacked gate vertical flash memory as claimed in claim 14, wherein the control gate conducting layer comprises a polysilicon layer or an epi-silicon layer.

25. The stacked gate vertical flash memory as claimed in claim 14, wherein the isolation layer comprises an oxide layer.

26. A method for fabricating a stacked gate vertical flash memory, comprising:

providing a semiconductor substrate, wherein a trench is formed in the semiconductor substrate;

conformally forming an isolation layer on a bottom of the trench;

forming a source conducting layer on the bottom of the trench, wherein the source conducting layer and the semiconductor substrate are separated by the isolation layer;

conformally forming an ion doped insulating layer on a sidewall of the trench and the source conducting layer;

annealing the ion doped insulating layer, wherein the dopant is driven in to the semiconductor substrate of the bottom of the trench to form a source area, the dopant is driven in the source conducting layer to form a common source area, and the source area and the common source area are connected;

removing the doped ion insulating layer;

forming an insulating layer on the source conducting layer, wherein the source conducting layer and

others formed thereon are separated by the insulating layer;

sequentially forming a gate dielectric layer and a conducting spacer on the sidewall of the trench, wherein the conducting layer covers the gate dielectric layer as a floating gate, and a top portion of the conducting spacer is a tip;

dopant implanting into the top of the conducting spacer to form a drain area on a side of the top of the conducting spacer in the semiconductor substrate;

forming an inter-gate dielectric layer covering the conducting layer; and

filling a control gate layer in the trench.

27. The stacked gate vertical flash memory as claimed in claim 26, wherein the source conducting layer comprises a polysilicon layer or an epi-silicon layer

28. The stacked gate vertical flash memory as claimed in claim 26, wherein the insulating layer comprises an oxide layer.

29. The stacked gate vertical flash memory as claimed in claim 26, wherein the gate dielectric layer comprises a gate oxide layer.

30. The stacked gate vertical flash memory as claimed in claim 26, wherein the conducting spacer comprises a polysilicon layer or an epi-silicon layer.

31. The stacked gate vertical flash memory as claimed in claim 14, wherein the dopant comprises As ions.

32. The stacked gate vertical flash memory as claimed in claim 26, wherein the inter-gate dielectric layer comprises a gate oxide layer.

33. The stacked gate vertical flash memory as claimed in claim 26, wherein the control gate conducting layer comprises a polysilicon layer or an epi-silicon layer.